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(54) Trench sidewall isolation by polysilicon oxidation

Seitenwandisolation für eine Grube mittels Oxidation von Polysilizium

Isolation de la paroi latérale d'une rainure utilisant l'oxydation de silicium polycristallin

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- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 28, no. 6, November 1985, pages 2583-2584, New York, US; "Trench filling process"**

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Description

BACKGROUND OF THE INVENTION

The invention relates to a method of forming semiconductor device isolation trenches and, more particularly, to a method of forming trenches having on the walls thereof a high integrity silicon dioxide insulator.

In integrated circuit (IC) technology it is usually necessary to isolate various active and passive devices in the IC. The preferred isolation is dielectric isolation because it allows butting of the circuit elements against the isolation and thereby result in greater density of packing of the active and passive devices on the IC chip. The art is replete with a variety of dielectric isolation schemes. Within the dielectric isolation arena, dielectric-filled trench isolation has received particular attention because of its ability to meet the basic requirements of an interdevice isolation of being efficient in electrical isolation and space utilization while maintaining good surface planarity. The overall process sequence of trench isolation fabrication consists of four basic process steps: (1) trench formation; (2) trench filling; (3) surface planarization; and (4) excess material removal. In this context, U.S. Patent 3,966,577 to Hochberg discloses a sputter etching method to achieve dielectric isolation using grown or deposited silicon dioxide to fill etched trenches.

IBM Technical Disclosure Bulletin, Vol. 21 (1), page 144, June 1977 by S. A. Abbas entitled "Recessed Oxide Isolation Process" describes a reactive ion etching (RIE) method to make recessed silicon dioxide filled trenches by partially filling the trenches with evaporated polysilicon material and then oxidizing the material.

U.S. Patent 4,104,086 to Bondur et al and assigned to the present assignee (which, incidentally, contains extensive citation of prior isolation techniques) teaches a method of achieving well-filled deep narrow grooves with near vertical walls by employing RIE. The method consists of the formation of slightly tapered narrow trenches cut through buried highly doped silicon regions, thermal oxidation of the trenches and proper filling-in of the remaining trenches with a vapor deposited dielectric material. This patent emphasizes the need for for forming slightly tapered walls and then addresses the dependency of the quality and planarity of the dielectric filling material on the trench taper angle and trench width. This patent also employs a back etching (by RIE) of the filling material which covers the total wafer to remove the material everywhere from the surface to leave only the isolation pockets.

U.S. Patent 4,139,442 to Bondur et al and assigned to the present assignee teaches a method of simultaneously making both shallow and deep recessed oxide isolation trenches. Shallow and deep trenches of equal narrow width are formed in the silicon substrate by RIE followed by thermally oxidizing the vertical trench walls to completely fill the trenches.

U.S. Patent 4,222,792 to Lever et al and assigned to the present assignee discloses a method of forming a deep wide dieletric-filled isolation trench. In this method a wide trench is formed in the surface of a silicon substrate, a thin oxide layer is formed on the trench walls by thermal oxidation of the trench and a layer of organic glass resin in a solvent is spin coated over the surface of the substrate and within the trench. The resin glass within the trench is exposed to an electron beam to render the glass within the trench impervious to a developing solvent. The remainder of the resin glass is stripped away by developing in a solvent, and the resin glass plug within the trench is converted to silicon dioxide by heating in an oxygen ambient. Finally, a layer of silicon dioxide is deposited over the entire surface of the substrate and etched away to planarize the trench.

IBM Technical Disclosure Bulletin Vol. 21 (4) pages 1466-1467, September 1978 entitled "Method of Etching/Filling Deep Trench Isolation for Large-Scale Integrated Devices" by Logan et al discloses use of magnesium oxide as a combination of etch mask and lift-off mask during oxide-filled trench fabrication. A trench is formed in a silicon substrate by RIE using MgO layer having a trench pattern. An oxide is grown on the exposed surfaces of the trench. The trench is filled by sputter depositing SiO2 to a depth less than the trench depth. The oxide sputtered in the device areas is removed by lift-off by dissolving the MgO layer.

U.S. Patent 4,238,278 to Antipov and assigned to the present assignee discloses forming deep and shallow trenches in a silicon substrate. Deep trenches are formed by RIE in the substrate. The trenches are partially filled with oxide by a combination of thermal oxidation of the trench surfaces and chemical vapor deposition (CVD). Filling of deep trenches is completed by the deposition of polysilicon to the surface level of the CVD oxide. Shallow trenches are then etched in the substrate and the exposed silicon and polysilicon corresponding to the shallow and deep trenches, respectively, is thermally oxidized.

U.S. Patent 4,356,211 to Riseman and assigned to the present assignee describes a method of forming air-dielectric isolation regions in silicon. Trenches are formed in the silicon substrate by RIE after having etched openings in an oxide-nitride dual layer on the substrate surface. The surfaces of the trenches are oxidized prior to depositing polycrystalline silicon on the trench sidewalls and on the walls defining the openings in the dual layer. By selectively doping the portion of the polysilicon on the walls of the openings in the dual layer so that this polysilicon will oxidize at a faster rate than the polysilicon on the trench walls, thermal oxidation causes the polysilicon to close in the upper end of each of the trenches while leaving an air space therebeneath to form the dielectric isolation regions.

U.S. Patent 4,544,576 to Chu et al and assigned to the present assignee discloses deep glass-filled trench isolation. After forming trenches in a silicon substrate by RIE, an oxide trench liner is grown. A glass having a co-

efficient of thermal expansion closely matching that of the substrate is deposited to entirely or partially fill the trench. The structure is then fired until the glass particles fuse into a continuous glass layer and final smoothing if necessary is accomplished.

U.S. Patent 4,571,819 to Rogers et al describes a method of forming oxide-filled trenches without leaving a void or insufficiently filled trench in the center of the trench. In this method, silicon dioxide trench fill containing 3-9 weight percent of N or P type dopant material is reflowed at 950-1150°C to collapse any voids therein and produce surface planarity. An underlaying oxide-polysilicon-nitride layer permits the formation and reflow of the doped oxide and remains in place in the trench.

U.S. Patent 4,509,249 describes a method of fabricating polysilicon-filled trench isolation. After forming a U-shaped groove in a silicon substrate by RIE and thermally oxidizing the trench surfaces to form a thick oxide, undoped polysilicon is deposited to fill the groove. The polysilicon material which is deposited on the substrate surface is etched off while simultaneously recessing the polysilicon in the groove followed by completion of groove filling with bias sputtered oxide.

With the advent of the very large scale integrated circuit and its requirement (due to low dopant concentrations in the substrate material) of establishing electrical contact to the substrate containing the IC at the top side rather than back side thereof for reverse biasing the substrate, filling of trenches with conductive material came into vogue. Doped polysilicon has been favored as the conductive trench fill because it gives rise to minimal crystallographic defect formation during the various subsequent thermal cycles owing to the excellent thermal expansion coefficient compatibility of the polysilicon with the silicon material. In this context IBM Technical Disclosure Bulletin, Vol. 25(2) pages 588-589, July 1982 by Antipov et al entitled "Post Emitter Polysilicon Trench Isolation" teaches use of doped polysilicon as the trench filling material. After forming all the elements of a bipolar device on a silicon substrate, using an oxide-nitride etch mask, a deep trench is formed in the substrate by RIE. The trench surfaces are oxidized to form a thin oxide layer, followed by deposition of a thin nitride layer. The oxide-nitride layers at the bottom of the trench are removed followed by deposition of doped polysilicon to fill the trench and establish substrate contact via the trench bottom. Excess polysilicon is removed followed by oxidation to convert the top portion of the polysilicon trench fill into a passivation layer.

IBM Technical Disclosure Bulletin, Vol.25(5), pages 2288-2291 by Anantha et al entitled "Method of Forming Polysilicon-Filled Regions in an Integrated Circuit Device" discloses a variation of the Antipov et al method where in the trench walls are coated with a CVD oxide and polysilicon trench fill material is recessed substantially below the substrate surface.

U.S. Patent 4,256,514 to Pogge and assigned to the present assignee discloses a process of forming in a silicon substrate deep and shallow oxide-filled trenches in conjunction with polysilicon-filled trenches, the latter for establishing electrical contact with the substrate from the top surface of the substrate. A CVD oxide layer formed on the walls of the polysilicon-filled trenches to provide the necessary dielectric isolation between devices IC.

IBM Technical Disclosure Bulletin Vol 28 n°6, pages 2583-2584 discloses a trench filling process in which the polysilicon layer on the trench sidewalls can be doped. In this process, the dopant diffuses into the polysilicon of the fill. It is also stated that outdiffusion of the dopant can be used to form a channel stop region at the trench bottom.

In trench isolation technology it is important that the trench liner and the trench-fill material be of high quality and integrity. Particularly in polysilicon-filled trench technology, since interdevice isolation is provided by the insulator layer (invariably, a thick oxide) on the sidewalls of the trench, while the doped polysilicon fill serves as the electrically conductive medium for biasing the substrate, it is imperative that the trench sidewall be of high integrity. However, the prior art methods of forming the trench sidewall oxide insulator, regardless of whether formed by CVD or thermal oxidation have basic shortcomings.

To elaborate on the above shortcomings, reference is made to Fig. 1 wherein is shown a deep trench coated with a CVD oxide. Numeral 10 designates a silicon substrate in which the trench is formed and 12 and 14 designate thin oxide and nitride trench liners, respectively. The CVD oxide sidewall is designated by 16 and the polysilicon fill, which is of the same conductivity type as the substrate 10, by 18. The CVD oxide sidewall insulator 16, although providing excellent conformality desired of a trench sidewall, suffers from susceptibility to erosion 20 at the top thereof during the wet (e.g., buffered hydrofluoric acid) etching steps associated with the excess material (invariably, a thermally grown oxide mask) removal step of trench fabrication mentioned hereinabove or with subsequent device fabrication. This erosion of the CVD oxide sidewall 16 occurs because the etch rate of CVD oxide is extremely high (typically, 5-6 times) compared to that of thermally grown oxide. As a result of this erosion, subsequent utilization of the substrate 10 leads to serious electrical shorting problems. For example, in state-of-the-art bipolar device fabrication wherein polysilicon base is defined such that it overlaps the trench, the doped polysilicon base material will fill the narrow grooves 22 forming conductive polysilicon rails embedded therein. This leads to base-to-isolation shorts and leakage through the doped polysilicon rails.

In addition to the vertical erosion during wet etching, the CVD sidewall oxide 16 is also susceptible to lateral erosion. Since the etch rate of the CVD oxide is inherently high, the various etching steps to remove the nitride 14 and oxide 12 from the trench bottom and trench cleaning steps prior to filling with polysilicon 18 tend to thin

down the CVD sidewall oxide 16 as indicated by numeral 24 in Fig. 1. Since the thickness of the sidewall insulator 16 is key to the capacitance associated with the trench (the thinner the insulator, the larger is the capacitance), thinning of the sidewall oxide 16 leads to unacceptable trench sidewall capacitance.

One way of minimizing the lateral erosion 24 (Fig. 1) and preserving the trench CVD sidewall oxide thickness is by providing protective layers. However, this adds to the complexity and cost of the trench fabrication process. Likewise, the erosion 20 at the top can be minimized by means of additional barrier layers (such as silicon nitride or sacrificial undoped polysilicon), but at the expense of additional cost and process complexity.

Turning to the shortcomings of the second prior art method of forming the sidewall oxide, viz., by thermal oxidation of the silicon trench, in this method, which involves covering the silicon substrate with an oxidation resistant trench-definition mask, RIE of the trench and a high temperature thermal oxidation of the trench surfaces, the grown oxide is sensitive to the dopant type and concentration variations in the substrate. For example, referring to Figs. 2A and 2B, wherein the substrate 30 is P type, contains a blanket N+ subcollector layer 32 of a high dopant concentration and an N type epitaxial silicon layer 34 of a lower dopant concentration than the N layer 32, uniform oxidation will not take place at the trench sidewalls. Referring to Fig. 2A, due to the higher dopant concentration in the subcollector layer 32, the trench portion corresponding to the layer 32 will undergo enhanced oxidation leading to a distortion 36 of the original trench wall profile. The subsequent etching step to remove the oxide at the trench bottom to facilitate substrate contacting, leads to pinholes, discontinuities and other defects in the oxide sidewall due to localized thinning thereof. Consequently, upon filling the trench with highly (P) doped polysilicon, the P dopant will outdiffuse into the substrate via the pinhole and other defects in the grown sidewall oxide causing the pinch-off defects 40. A similar pinch-off defect 42 will occur, as illustrated in Fig. 2B, at the top of the trench near the interface between the epitaxial layer 34 and the trench-definition mask (not shown) due to thinning of sidewall oxide 44 at the top corners of the trench during the etch steps to remove the oxide 44 at the trench bottom and the trench-definition mask. The pinch-off defects 40 and 42 result in a low isolation breakdown.

The invention solves these and other problems by a novel process which is simple and straight-forward.

It is an object of the invention to provide a high integrity oxide sidewall for trench isolation to alleviate the low trench isolation breakdown characteristic of the prior art.

It is another object of the invention to provide a trench sidewall oxide which exhibits the conformality of a CVD oxide and the etch resistance of thermally grown oxide.

As used herein the phrase "polysilicon oxide" means oxide obtained by a complete thermal oxidation of polysilicon.

SUMMARY OF THE INVENTION

In accordance with the general concept of the invention, a process of forming an isolation trench in a P-type semiconductor is given by claim 1. Additional features are given in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features, individual process steps and their combination which are characteristic of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the detailed description which follows in conjunction with the accompanying drawings wherein:

Fig. 1 is cross-sectional representation of a prior art trench isolation structure wherein the trench sidewall oxide is formed by CVD showing the deficiencies of the prior art.

Figs. 2A and 2B illustrate in a cross-sectional representation a prior art trench structure wherein the trench sidewall oxide is formed by thermal oxidation showing the shortcomings of the prior art.

Figs. 3-8 are flow diagrams illustrating by sequential cross-sectional representation a process for forming a trench isolation structure having polysilicon oxide sidewall.

Figs. 9-11 are cross-sectional representations of forming a trench isolation structure having polysilicon oxide sidewall using the process of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring to the Figs. 3-8, a process for forming a trench isolation structure will be described. As illustrated in Fig. 3, starting with a P type silicon substrate 50, a triple layer mask consisting of about 150-200 nm thick silicon dioxide 52, about 80-120 nm thick silicon nitride 54 and about 500-1000 nm thick CVD oxide 56 is formed. The oxide 52 serves as a pad to buffer the stress induced by the nitride 54 on the substrate 50. The nitride serves as an oxidation mask during a later stage of the present fabrication process. The CVD oxide 56, serves, among other things as a mask during the trench etching step.

In the following description a P type silicon substrate is used. The thickness of the various layers may also be altered as desired, depending on the device design. It will also be understood that the substrate material is not limited to silicon. The process can be applied to other

semiconductor substrates for fabricating trench isolation. Also, the drawings are not to scale. The thickness of the various layers are shown for clarity of illustration.

The triple layer 52-54-56 mask is patterned in accordance with the desired trench pattern using conventional lithographic and etching techniques. A trench pattern is then formed in substrate 50 by RIE. Details of the trench etching process are contained in the aforementioned Bondur et al patent No. 4,104,086 which is hereby incorporated by reference herein. For convenience of illustration, only a part of the trench pattern consisting of a single trench 58 is shown in Fig. 3. The trench 58 for device isolation purposes is sufficiently deep and narrow, typically, in the range 1-5 µm and consists of substantially vertical walls 60 and a substantially horizontal floor 62. Next, a high quality surface oxide 64 lining the trench walls is formed to assure a good silicon to silicon dioxide interface with low surface state densities. Oxide 64 is typically about 50-70 nm thick and is formed by thermal oxidation of the trench.

Progressing toward the structure of Fig. 4, a uniformly thick and conformal polysilicon layer 66 is formed by CVD on all the trench surfaces including the oxide-coated vertical and horizontal surfaces 60 and 62, respectively, and on the CVD oxide mask 56. The thickness of the polysilicon layer 66 is adjusted to be equal to approximately 40% of the desired thickness of the trench oxide sidewall, which,in turn, is governed by the collector-base capacitance required of the isolation structure. Typically, the polysilicon 66 thickness is in the range of about 100-150 nm. LPCVD is a preferred method of forming polysilicon 66 since this provides a better conformal coating. Polysilicon 66 is deposited by the pyrolysis of a silicon-bearing gas such as silane and dichlorosilane, typically, in the temperature range 600-800°C in an atmospheric pressure system or reduced pressure system at a low pressure of about 13,3-26,6 Pa (100-200 milli torr).

In the next process step, which is illustrated in Fig. 5, the polysilicon 66 is subjected to thermal oxidation to completely convert the polysilicon into a polysilicon oxide 68. Steam oxidation at a temperature of about 900-1000°C is employed for this conversion process. Since the silicon source giving rise to the polysilicon oxide 68 is a conformal (polysilicon) layer (66), the oxide 68 will be correspondingly conformal as well. Also, since the polysilicon oxide 68 is obtained by thermal conversion of polysilicon (66), the etch characteristics of the oxide 68 will be as superior as that of oxide grown by thermal oxidation of silicon. The polysilicon oxide 68 will additionally have a high quality which, in conjunction with the oxide liner 64 (which is not shown in Fig. 5 since it is indistinguishable from oxide 68), provides an excellent interface with low surface state densities between the vertical surfaces 60 and horizontal surface 62 of silicon 50 and oxide 68. Thus, by forming a CVD polysilicon as a precursor to the trench sidewall oxide and thermally converting the precursor polysilicon into oxide, a trench sidewall is obtained which exhibits both the conformality of a CVD oxide layer and the high etch resistance of a thermally grown oxide.

The next process step is filling of trench 58. The trench may be filled with any of several different materials. In the case of device applications, the filling material is some form of dielectric material, such as oxides, polymers, epitaxial silicon or polycrystalline silicon. The trench may also be filled with a conductive metal to obtain buried interconnecting device lines.

If contact to substrate 50 is desired, the oxide 68 corresponding to the bottom 62 of the trench 58 needs to be removed prior to filling the trench with a conductive material. This removal is accomplished by vertical RIE using, for example, CF4 etchant gas species. During this RIE step, the oxide 68 formed on the surface of CVD oxide mask 56 is also removed leaving sidewall oxide 68' on the vertical walls of the trench. Next, to ensure that the P type substrate 50 does not invert during the subsequent processing and cause device-to-device leakages, implantation of the trench with P type (e.g., boron) ions may be accomplished. The implant is directed vertically into the trench. Under these conditions, the trench sidewall oxide 68' acts as an efficient mask while the implant in the bottom can reach into the substrate and form a P+ region 72.

The above trench implantation step is avoided and yet the P region 72 is formed thereby obtaining process cost savings. In this process trench 58 is filled by CVD of in-situ P doped polysilicon 70. Boron is typically used as the dopant for this purpose. CVD of polysilicon is preferred since it facilitates conformal coating, excellent control of the deposition and generally prevents formation of voids in the trench fill. The polysilicon deposition temperature is about 900-1000°C and the deposition pressure is about an atmosphere. The polysilicon 70 deposition is continued until a thick (2-3 µm) surface layer thereof is formed on the substrate covered by mask 56. During the polysilicon 70 deposition step, due to the high temperature of deposition, some of the P-type dopant from the polysilicon 70 will diffuse a sufficient depth into the substrate via the trench bottom 62 into the substrate 50 thereunder forming the highly doped P+ channel stop. Thus, in a single process step according to the invention, polysilicon 70 trench filling, doping of the trench fill 70 (to a high concentration level) with the same conductivity type dopant as the substrate and diffusion of this dopant into the substrate directly beneath the trench to form the P+ region 72 are accomplished.

Having completed filling the trench, next as illustrated in Fig. 7, planarization of the substrate surface is accomplished using well-known planarization techniques to remove excess polysilicon 70, i.e. the polysilicon 70 above the level of the surface of substrate 50. Chemical-mechanical polishing may be used to remove the portion of the excess polysilicon 70 above the surface of the nitride layer 54. During this step, the CVD oxide 56 will also be removed and the nitride 54 serves as a

polish-stop indicator. The polysilicon trench fill may be recessed, by a suitable etching step such as RIE, below the surface of the substrate 50 followed by subjecting to a thermal oxidation step at a suitable temperature to passivate the top of the trench. Thermal oxidation converts the top portion of the polysilicon trench fill 70' into polysilicon oxide 74, while the remainder of the substrate is protected by the oxidation-resistant nitride 54 mask. The nitride 54 is removed by a wet etching using, for example, hot phosphoric acid. The thermal oxide mask 52 is next removed by either wet etching or dry etching. During the oxide 52 removal step, a surface portion of the polysilicon oxide 74 and an upper portion of the trench sidewall oxide 68'is also removed to a certain extent. However, since the sidewall polysilicon oxide 68' has a high etch resistance (equal to that of the thermal oxide 52) there will be no erosion of the oxide 68' (during the wet etching steps) like was typical in the prior art. The resulting structure, shown in Fig. 8, consists of a trench 58 filled with P+ doped polysilicon 70' having a polysilicon oxide cap 74 and high-integrity sidewall polysilicon oxide 68'. To establish electrical contact with the substrate 50, the oxide cap 74 is selectively opened up using conventional lithography and etching and metallization in contact the P+ polysilicon fill 70' is formed.

An embodiment of the fabrication process of the present invention of forming an isolation trench having a high integrity sidewall oxide, is illustrated in Figs. 9-11. Referring to Fig. 9, in particular, after forming the barrier oxide 60 on the vertical and horizontal surfaces of the trench 58 analogous to that described in connection with the Fig. 3 structure formation, a thin (typically, 50-150 nm thickness) silicon nitride layer 80 is deposited. The nitride 80 will later on serve as an etch stop during polysilicon removal. After forming the nitride 80, undoped polysilicon layer 82 is deposited. The process of forming and the characteristics of the polysilicon 82 are quite similar to those of polysilicon layer 66 described in connection with Fig. 4.

Turning now to the structure of Fig. 10, the polysilicon layer 82 in correspondence with the horizontal surface 62 of the trench 58 and that overlying the horizontal portion of the nitride 80 are removed by vertical RIE. CF4 RIE is preferred. The resulting structure, shown in Fig. 10, will have polysilicon sidewalls 82' in correspondence with only the vertical surfaces 60 of the trench 58. Next, by thermal oxidation in steam at a temperature of 900-1100°C, the polysilicon 82' is completely converted to polysilicon oxide sidewalls 84 as indicated in Fig. 11. During the thermal conversion of the polysilicon 82' into polysilicon oxide 84 the volume expansion of the polysilicon takes place in a single direction, i.e., perpendicular to the vertical surfaces 60 of the trench 58, the stress created on the substrate 50 (particularly the corners of the trench) by the oxide 84 will be minimal. Minimization of this stress translates into minimization of formation and/or propagation of crystalline defects such as dislocations in the silicon material 50. Thus, by forming, in a tailor-made fashion, the (poly) silicon source solely on the vertical surface of the trench and obtaining from the silicon source an oxide layer, numerous benefits are gained. A trench sidewall oxide 84 is obtained precisely where desired. The oxide 84 has an etch rate matching that of thermally grown oxide and conformality of CVD oxide.

Crystalline defects in the silicon substrate are kept at a minimum despite formation of a thick trench sidewall oxide 84.

After forming the polysilicon oxide 84 as shown in Fig. 11, if substrate contact is desired, the oxide 64 and nitride 80 corresponding to the trench bottom 64 is removed by RIE. The remainder of the process including trench filling, planarization and excess material removal corresponds to that described hereinabove in connection with Figs. 6-8.

A split lot experiment comparing the frequency of breakdown of trench sidewall oxide formed by prior art thermal oxidation process with that formed by the present polysilicon oxidation process demonstrated significant results. The thickness of the sidewall oxide in both cases was the same, approximately 300 nm. Using one lot of wafers, the polysilicon sidewall oxide was formed by growing a 50 nm thick oxide barrier in the RIE-defined silicon trenches; depositing about 120 nm thich polysilicon layer; and oxidizing the polysilicon into polysilicon oxide. In the second lot of wafers the thermal oxide was formed by straight-forward thermal oxidation of the RIE-defined trenches. Sidewall etching, P+ polysilicon trench filling and planarization were common to both lots of wafers. Breakdown voltage measurement on the sidewall oxide demonstrated that the polysilicon oxide sidewall structures generally have a significantly lower failure rate than that of the thermal oxide sidewall structures.

Thus, there has been provided, in accordance with the invention a process of growing a high-integrity thermal oxide on a non-oxidizable surface that fully satisfies the objectives and advantages set forth above.

While the invention has been described in conjunction with a specific preferred embodiment, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description. While the invention has been described in conjunction with filling trenches with polysilicon, it is readily adaptable for forming epitaxial filled trenches.

Claims

1. A process of forming an isolation trench (58) in a P-type semiconductor substrate (50) comprising:

   a) providing said P-type semiconductor substrate (50) covered with an insulator layer (52, 54, 56);

b) forming said trench (58) having substantially vertical surfaces (60) and a substantially horizontal surface (62) in said substrate by etching an opening in said insulator layer followed by etching the underlying substrate in correspondence with said opening;

c) thermally oxidizing said trench to form a thin oxide trench liner (64) on said surfaces;

d) depositing a layer of silicon nitride (80) on said oxide trench liner;

e) depositing a conformal layer of polysilicon (82) on said surfaces of the trench and on said insulator layer;

f) removing said polysilicon from said horizontal surface ;

g) thermally oxidizing to completely convert said polysilicon into a polysilicon oxide layer (84);

h) removing by RIE said oxide liner (64) and said silicon nitride layer (80) from said horizontal surface corresponding to the said trench bottom to expose said semiconductor substrate ; and,

i) depositing by chemical vapour deposition at a high temperature in the range 900-1000°C a layer of doped polysilicon (70) having a high concentration of P-type dopant to form a thick doped polysilicon layer atop said insulator and to simultaneously fill the trench and form a highly doped P+ channel stop (72) at the bottom of said trench by the diffusion of said dopant from said doped polysilicon (70) into the exposed substrate.

2. The process as in claim 1 step b) wherein the step of etching an opening in said insulator is achieved by wet etching.

3. The process as in claim 1 wherein the step i) of doped polysilicon deposition is achieved by low pressure chemical vapor deposition.

4. The process as in claim 1 further comprising:

j) etching to remove said thick doped polysilicon layer (70) above the level of the substrate and recessing said doped polysilicon filling said trench, utilizing said nitride layer (80) as an etch mask;

k) thermally oxidizing the upper portion of said recessed polysilicon filling said trench to form a polysilicon oxide cap (74); and,

l) removing said insulator layer (52, 54, 56) by wet etching while maintaining intact said polysilicon oxide layer (84) on the trench walls near the substrate surface.

Patentansprüche

1. Verfahren zur Bildung eines Isolationsgrabens (58) in einem p-leitenden Halbleitersubstrat (50), das umfaßt:

a) Bereitstellen des p-leitenden Halbleitersubstrats (50), das mit einer Isolatorschicht (52, 54, 56) bedeckt ist;

b) Erzeugen des Grabens (58) mit im wesentlichen vertikalen Oberflächen (60) und einer im wesentlichen horizontalen Oberfläche (62) in dem Substrat durch Ätzen einer Öffnung in die Isolatorschicht, gefolgt von einem Ätzen des darunterliegenden Substrates entsprechend der Öffnung;

c) thermisches Oxidieren des Grabens, um eine dünne Grabenzwischenlage (64) aus Oxid auf den Oberflächen zu bilden;

d) Aufbringen einer Schicht aus Siliciumnitrid (80) auf der Grabenzwischenlage aus Oxid;

e) Aufbringen einer konformen Schicht aus Polysilicium (82) auf den Oberflächen des Grabens und auf der Isolatorschicht;

f) Entfernen des Polysiliciums von der horizontalen Oberfläche;

g) thermisches Oxidieren, um das Polysilicium vollständig in eine Polysiliciumoxidschicht (84) umzuwandeln;

h) Entfernen der Oxidzwischenlage (64) und der Siliciumnitridschicht (80) von der dem Grabenboden entsprechenden horizontalen Oberfläche durch RIE, um das Halbleitersubstrat freizulegen; und

i) Aufbringen einer Schicht aus dotiertem Polysilicium (70) mit einer hohen Konzentration eines p-leitenden Dotierstoffes durch chemische Gasphasenabscheidung bei einer hohen Temperatur im Bereich von 900 °C bis 1000 °C, um eine dicke dotierte Polysiliciumschicht oben auf dem Isolator zu erzeugen und um gleichzeitig den Graben zu füllen und einen hoch p^+-dotierten Kanalstopp (72) am Boden des Grabens durch die Diffusion des Dotierstoffes

von dem dotierten Polysilicium (70) in das freigelegte Substrat zu bilden.

2. Verfahren wie in Anspruch 1, Schritt b), wobei der Schritt des Ätzens einer Öffnung in den Isolator durch Naßätzen erzielt wird.

3. Verfahren wie in Anspruch 1, wobei der Schritt i) der Deposition von dotiertem Polysilicium durch chemische Gasphasenabscheidung bei niedrigem Druck erzielt wird.

4. Verfahren wie in Anspruch 1, das des weiteren umfaßt:

j) Ätzen, um die dicke dotierte Polysiliciumschicht (70) oberhalb des Substratniveaus zu entfernen, und Vertiefen des dotierten Polysiliciums, das den Graben füllt, wobei die Nitridschicht (80) als Ätzmaske verwendet wird;

k) thermisches Oxidieren des oberen Teils des vertieften Polysiliciums, das den Graben füllt, um eine Abdeckung (74) aus Polysiliciumoxid zu bilden; und

l) Entfernen der Isolatorschicht (52, 54, 56) durch Naßätzen, während die Schicht (84) aus Polysiliciumoxid auf den Grabenwänden nahe der Substratoberfläche intakt gehalten wird.

Revendications

1. Processus de formation d'une tranchée d'isolation (58) dans un substrat en semi-conducteur de type P (50) comprenant les étapes consistant à :

a) procurer ledit substrat semi-conducteur de type P (50) recouvert d'une couche d'isolation (52, 54, 56),

b) former ladite tranchée (58) présentant des surfaces pratiquement verticales (60) et une surface pratiquement horizontale (62) dans ledit substrat par gravure d'une ouverture dans ladite couche d'isolation suivie d'une gravure du substrat sous jacent en correspondance avec ladite ouverture,

c) oxyder de façon thermique ladite tranchée afin de former un fin revêtement de tranchée en oxyde (64) sur lesdites surfaces,

d) déposer une couche de nitrure de silicium (80) sur ledit revêtement de tranchée en oxyde,

e) déposer une couche conforme de silicium polycristallin (82) sur lesdites surfaces de la tranchée et sur ladite couche d'isolation,

f) enlever ledit silicium polycristallin de ladite surface horizontale,

g) oxyder de façon thermique afin de transformer complètement ledit silicium polycristallin en une couche d'oxyde de silicium polycristallin (84),

h) enlever à l'aide d'une attaque par ions réactifs ledit revêtement d'oxyde (64) et ladite couche de nitrure de silicium (80) de ladite surface horizontale correspondant audit fond de tranchée afin d'exposer ledit substrat semi-conducteur, et

i) déposer par dépôt chimique en phase vapeur à une température élevée dans la plage de 900 à 1000°C, une couche de silicium polycristallin dopée (70) présentant une concentration élevée de dopant de type P afin de former une couche de silicium polycristallin dopée épaisse au-dessus de ladite isolation et afin de remplir simultanément la tranchée et former un arrêt de canal P+ dopé fortement (72) au fond de ladite tranchée par la diffusion dudit dopant à partir dudit silicium polycristallin dopé (70) dans le substrat exposé.

2. Processus selon la revendication 1 étape b) dans lequel l'étape de gravure d'une ouverture dans ledit isolant est réalisée par gravure humide.

3. Processus selon la revendication 1 dans lequel l'étape i) du dépôt de silicium polycristallin dopé est réalisé par un dépôt chimique en phase vapeur à basse pression.

4. Processus selon la revendication 1 comprenant en outre :

j) une gravure pour enlever ladite couche de silicium polycristallin dopée épaisse (70) au-dessus du niveau du substrat et évider ledit silicium polycristallin remplissant ladite tranchée,

k) l'oxydation thermique de la partie supérieure dudit silicium polycristallin évidé remplissant ladite tranchée afin de former une coiffe d'oxyde de silicium polycristallin (74), et

l) l'enlèvement de ladite couche d'isolant (52, 54, 56) par une gravure humide, tout en maintenant intacte ladite couche d'oxyde de silicium polycristallin (84) sur les parois de tranchées à proximité de la surface du substrat.

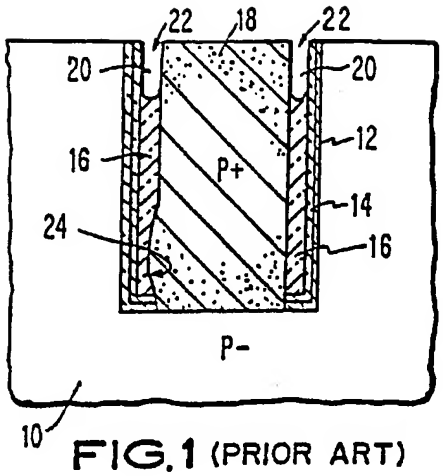

FIG. 1 (PRIOR ART)

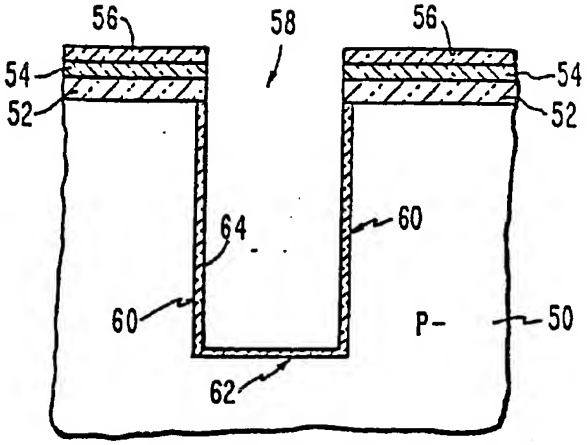

FIG. 3

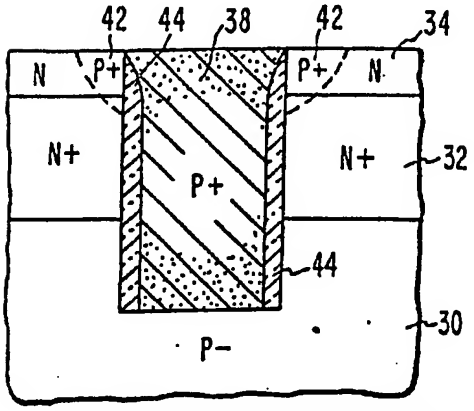

FIG. 2B (PRIOR ART)

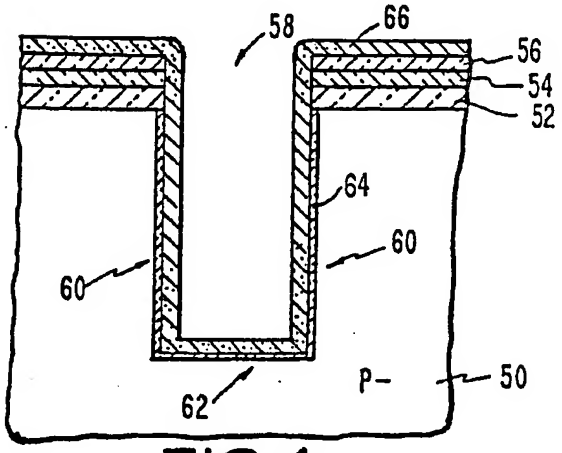

FIG. 4

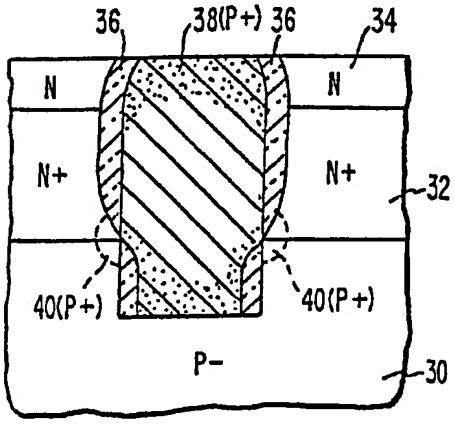

FIG. 2A (PRIOR ART)

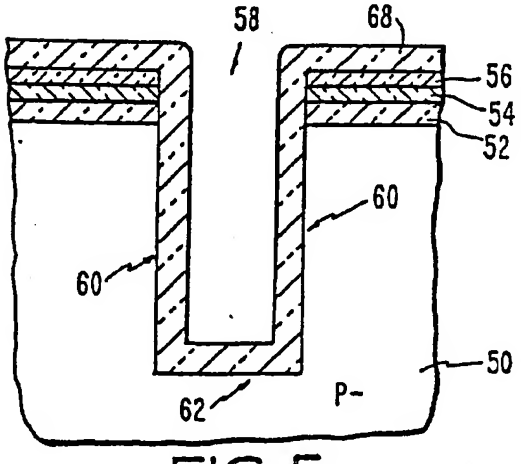

FIG. 5

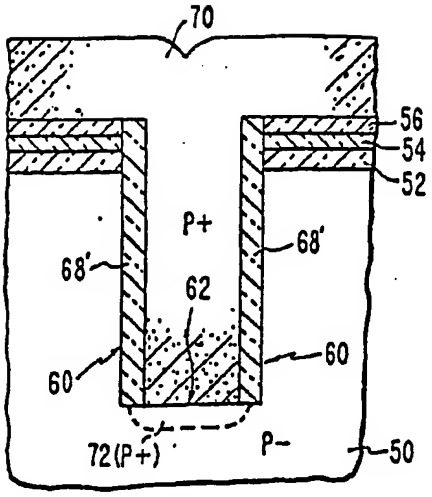

FIG. 6

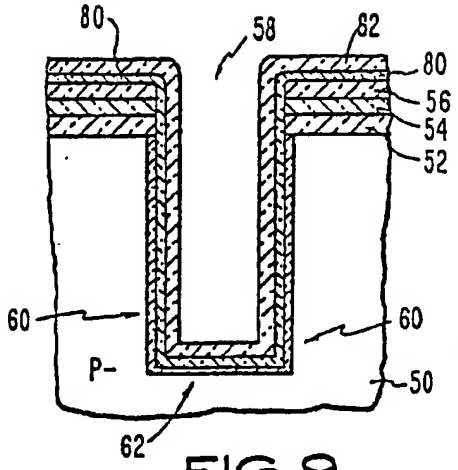

FIG. 9

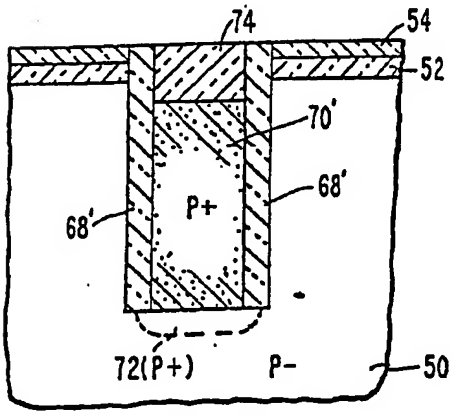

FIG. 7

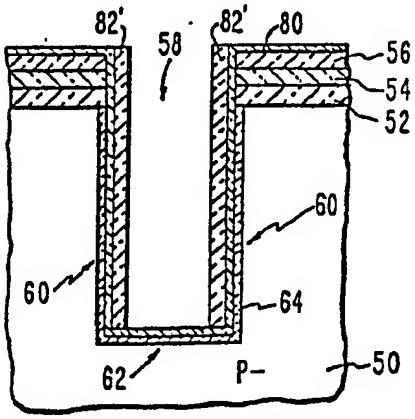

FIG. 10

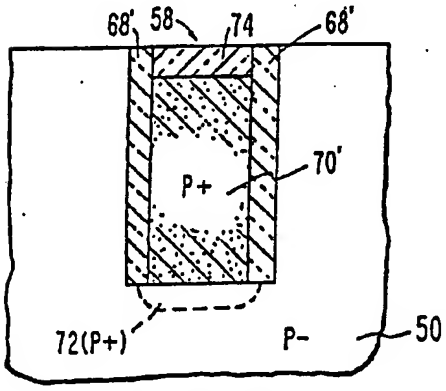

FIG. 8

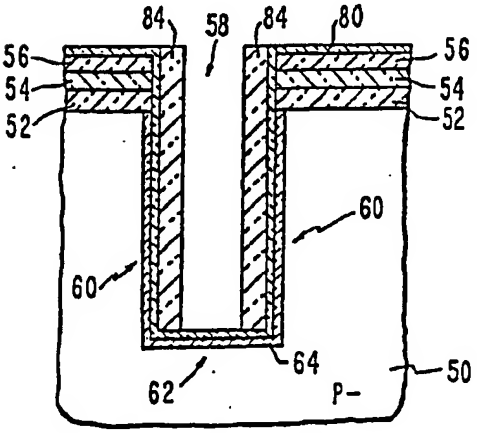

FIG. 11

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